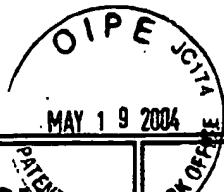




MAY 21 2004

SHEET 1 OF 1

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).



MAY 19 2004

SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION PTO-1449		PATENT & TRADE MARK OFFICE	ATTORNEY'S DKT No. H1492	APPLICATION No. 10/653,105
		Customer Number 26615	APPLICANT(S) Bin Yu et al.	FILING DATE September 3, 2003
				GROUP 2 <u>Unassigned</u>

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
<u>W</u>	EP 0 623 963 A1	11-09-94	Europe	—	—		X

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

✓	PCT International Search Report, April 8, 2004, 3 pages.

EXAMINER

HUNG VU

DATE CONSIDERED

08/07/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

INFORMATION DISCLOSURE CITATION PTO-1449		Customer Number: 26615	ATTORNEY'S DKT NO. H1492	APPLICATION NO. Unassigned 10/653,105		
			APPLICANT(S) Bin Yu et al.			
			FILING DATE September 3, 2003	GROUP 2811 Unassigned		
U.S. PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
<u>Vu</u>	6,525,403 B2	02-25-03	Inaba et al.	257	618	09-24-01/
<u>Vu</u>	6,433,609 B1	08-13-02	Voldman	327	313	11-19-01
FOREIGN PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes No
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)						
<u>Vu</u>	Digh Hisamoto et al.: "FinFET - A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.					
	Yang-Kyu Choi et al.: "Sub-20nm CMOS Fin FET Technologies," 2001 IEEE, IEDM, Pages 421-424.					
	Xuejue Huang et al.: "Sub-50 nm P-Channel Fin FET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.					
	Yang-Kyu Choi et al.: "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.					
	Xuejue Huang et al.: "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.					
	Co-pending Application Serial No. 10/348,758, filed January 23, 2003, entitled "GERMANIUM MOSFET DEVICES AND METHODS FOR MAKING SAME," 22 page specification, 29 sheets of drawings.					
	Co-pending Application Serial No. 10/274,961, filed October 22, 2002, entitled "DOUBLE AND TRIPLE GATE MOSFET DEVICES AND METHODS FOR MAKING SAME," 15 page specification, 12 sheets of drawings.					
	Co-pending Application Serial No. 10/348,911, filed January 23, 2003, entitled "TRI-GATE AND GATE AROUND MOSFET DEVICES AND METHODS FOR MAKING SAME," 17 page specification, 18 sheets of drawings.					
	U.S. Patent Application Publication No. US 2003/0113970 A1; June 19, 2003; Fried et al.					
<u>Vu</u>	U.S. Patent Application Publication No. US 2003/0042531 A1; March 6, 2003; Lee et al.					
EXAMINER	<u>HUNG VU</u>		DATE CONSIDERED 08/07/04			

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).